Please amend the application as follows:

In the drawings:

Please amend Figs. 1, 2, 3, 4, 10, 19 and 20 as indicated in red on the enclosed copies of these figures.

In the specification:

Please amend the paragraph starting on page 8 line 20 as follows:

The present invention provides for an improved multi-chip module having increased chip density over conventional modules presently in use. All embodiments of the improved module include a circuit board having an array of electrical interconnection pads to which are mounted a plurality of IC package units. Each IC package unit includes a package carrier having multiple IC packages, which are mounted on opposite sides of the package carrier. The package units may be mounted on one or both sides of the circuit board. The connection elements (leads or pads) of each of the packages are coupled to a carrier interface, which may or may not include discrete carrier leads. The carrier interface includes conductive links 111 between the mounting pads 103 on opposite sides of the package carrier within the package carrier as indicated with two examples in Fig. 1. Naturally, each set of opposing pads would be connected within carrier 101 in some similar fashion.

Please amend the second paragraph starting on page 9 at line 10 as follows:

Referring now to Figure 3, multiple first embodiment package units 201 (in this example, four) are shown ready for mounting on a circuit board 301. In this example, two package units 201A and 201B will be mounted on the upper surface 302U of the circuit

board 301, while two package units 201C and 201D will be mounted on the lower surface 302L thereof. One IC package 105H of each package unit 201 fits within its own recess 303 in the circuit board 301 so that it is completely hidden from view, while the other IC package 105E is completely exposed. The surrounding edges of each recess are equipped with a set of board electrical connection contact pads 304. The leads of each hidden package 105H will make direct contact with the contact pads of its recess and will be routed within the circuit board 301 to the appropriate interconnection sites. The leads 104 of the exposed IC package 105E are coupled to the leads 104 of the connections, which penetrate the laminar carrier 101. By using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example hidden package 105H by means of, if both packages are identical memory chips requiring individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 101 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 101. The circuit board 301 may incorporate one or more heat-sink layers 305 with which the bodies of hidden IC packages 105H are in surface-to-surface contact, either directly or indirectly via a thin layer of thermally-conductive paste, such as zinc oxide paste (not shown).

Please amend the paragraph starting on page 10 line 9 as follows:

Referring now to Figure 4, surface mounting of the package units 201 on the circuit board 301 has resulted in a completed first embodiment module 401. A cross sectional view through the plane ABCD 402 provides the view of Figure 5. As is well known in the art and schematically shown in Fig. 5 an integrated circuit chip 107 is typically imbedded in a carrier body 106.